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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,444	01/04/2002	Fumikazu Yamaki	011796	3015

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EXAMINER	
TRAN, TAN N	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 12/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/035,444	YAMAKI ET AL.
	Examiner	Art Unit
	TAN N TRAN	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. If applicant is aware of any relevant prior art, he/she requested to cite it on form PTO-1449 in accordance with the guidelines set forth in M.P.E.P. 609.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the compound semiconductor substrate comprising a compound semiconductor support substrate having a resistivity more than 1.0×10^8 Ohm-cm and a compound semiconductor having resistivity less than 1.0×10^8 Ohm-cm as recited in claim 11 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled

in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification does not disclose the compound semiconductor substrate comprising a compound semiconductor support substrate having a resistivity more than 1.0×10^8 Ohm-cm and a compound semiconductor having resistivity less than 1.0×10^8 Ohm-cm as recited in amended claim 11.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 5, line 2,3, "the electrode layer is not electrically connected to semiconductor device" is unclear. How the lower electrode formed on another surface of the substrate can be not electrically connected to the semiconductor device? Applicant's fig.12 shows electrode 25 is in ohmic contact with the substrate 21.

Claim Objections

5. Claims 6-10 are objected to because of the following informalities:

In claims 2-11, line 1, "A semiconductor device" should be changed to – The semiconductor device --.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being anticipated by Nitta (5,798,537) in view of Usagawa et al. (5,373,191).

With regard to claims 1,2, Nitta discloses a semiconductor device comprising a compound semiconductor substrate 100 having a resistivity less than 1 Ohm-cm at least at surface thereof, a buffer layer 101 formed on the compound semiconductor substrate 100; and an active layer 103 formed on the buffer layer 101 and having an active element (e.g. pn junction 104/102) formed therein. (Note lines 26-28, column 5, figs. 1, 2 of Nitta).

Nitta does not disclose the buffer layer having a supper lattice structure.

However, Usagawa et al. discloses the buffer layers (8,9) having a supper lattice structure formed on the compound semiconductor substrate 100. (Note lines 49,50, column 8, fig. 8a of Usagawa et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the buffer layer of Nitta's device having a supper lattice structure such as taught by Usagawa et al. in order to prevent the lattice mismatch between the substrate and the epitaxial layers formed above the substrate.

With regard to claim 3, Nitta and Usagawa et al. disclose all the claimed subject matter except for the active layer is formed at a position within 5.0 micrometer from a surface of the compound semiconductor substrate. However, it would have been obvious to one of ordinary skill in the art to form the active layer is formed at a position within 5.0 micrometer from the surface of the compound semiconductor substrate in order to maintain the lattice matching between the semiconductors and the sapphire substrate.

With regard to claims 4,5 Nitta discloses an electrode 106 formed on another surface of the compound semiconductor substrate 100. (Note fig. 2 of Nitta).

With regard to claim 6, Nitta and Usagawa et al. disclose all the claimed subject matter except for the electrode layer is connected to one power supply potential of the semiconductor device. However, it would have been obvious to one of ordinary skill in the art to connect the lower electrode layer to one power supply potential of the semiconductor device in order for the device to operate.

With regard to claim 7, Nitta does not disclose a source electrode and a drain electrode formed on the active layer, separated from each other so as to establish a channel region, and a gate electrode formed above the channel region.

However, Usagawa et al. discloses a source electrode 32 and a drain electrode 33 formed on the active layer 1, separated from each other so as to establish a channel region, and a gate electrode 30 formed above the channel region. (figs. 6a, 6b of Usagawa et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Nitta's device having a source electrode and a drain electrode formed on the active layer, separated from each other so as to establish a channel region, and a gate electrode formed above

the channel region such as taught by Usagawa et al. in order to obtain lower the parasitic resistance between the gate electrode and another electrode of the field effect transistor.

With regard to claim 8, Usagawa et al. discloses the active layer has 2 dimentional electron gas. (Note lines 34,35, column 11 of Usagawa et al.).

With regard to claim 9, Nitta does not disclose the active layer comprises: a collector layer of a first conducting type; a base layer of a second conducting type formed on the collector layer; an emitter layer of the first conducting type formed on the base layer.

However, Usagawa et al. discloses the active layer comprises: an n-type collector layer 101, a p-type base layer 103, and an n-type emitter layer 105. (Note figs. 12a-12c and embodiment 6 in column 10 of Usagawa et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Nitta's device having the active layer comprises: an n-type collector layer, a p-type base layer, and an n-type emitter layer such as taught by Usagawa et al. in order for forming the bipolar transistor.

Allowable Subject Matter

7. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 10 is allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as the compound semiconductor substrate has a resistivity more than 1.0×10^8 Ohm-cm in total.

Conclusion

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

Dec 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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